REMARKS

Claims 1, 2, 5, 7, 10 and 11 are now present in this application.

The specification and claims 1 and 7 have been amended and claims 3, 4, 6, 8 and 9 have been cancelled without prejudice or disclaimer of the subject matter contained therein. Reconsideration of the application, as amended, is respectfully requested.

OBJECTION TO THE DISCLOSURE

The disclosure stands objected to for certain informalities. In view of the foregoing amendments, in which the Examiner's helpful suggestions have been followed, it is respectfully submitted that these informalities have been addressed. Reconsideration and withdrawal of any objection to the specification are respectfully requested.

REJECTION UNDER 35 USC 112

Claim 6 stands rejected under 35 USC 112, second paragraph. This rejection is respectfully traversed.

In view of the foregoing amendments, in which claim 6 has been cancelled, this rejection is rendered moot.

REJECTION UNDER 35 USC 102(E)

Claims 1-11 stand rejected under 35 USC 102(e) as being anticipated by HURLEY et al., U.S. Publication No. 2002/0130357. This rejection is respectfully traversed.

Independent claim 1 recites limitations of "a polycide layer, formed on the tunneling dielectric layer" and "a plurality of polycide spacers, formed on the sidewalls of the polycide layer".

The polycide layer and the polycide spacers according to independent claim 1 are provided to improve the conductivity of the floating gate and reduce the contact resistance, which is critical for high frequency and submicron regime application. However, HURLEY et al. does not teach or suggest that the floating gate is formed by polycide. For example, HURLEY et al. teaches that the floating gate is a polysilicon layer in paragraph [0059], but the polycide floating gate is not contemplated by HURLEY et al.

With regard to independent claim 7, this claim recites limitations of "a polycide layer, formed on the tunneling dielectric layer" and "a plurality of polycide spacers, formed on the sidewalls of the polycide layer".

The polycide layer and the polycide spacers according to independent claim 7 are provided to improve the conductivity of the floating gate and reduce the contact resistance, which is critical for high frequency and submicron

regime application. However, HURLEY et al. does not teach or suggest that the floating gate is formed by polycide. For example, HURLEY et al. teaches that the floating gate is a polysilicon layer in paragraph [0059], but the polycide floating gate is not contemplated by HURLEY et al.

In view of the foregoing amendments and remarks, it is respectfully submitted that the floating gate having improved coupling ratio in independent claims 1 and 7, as well as their dependent claims, is neither taught nor suggested by the prior art utilized by the Examiner. Accordingly, reconsideration and withdrawal of the 35 USC 102(e) rejection are respectfully requested.

CONCLUSION

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By James T. Eller, Jr. #39,538
Joe McKinney Muncy, #32,334

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

KM/asc/te
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